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Fig. 1  
(Prior Art)

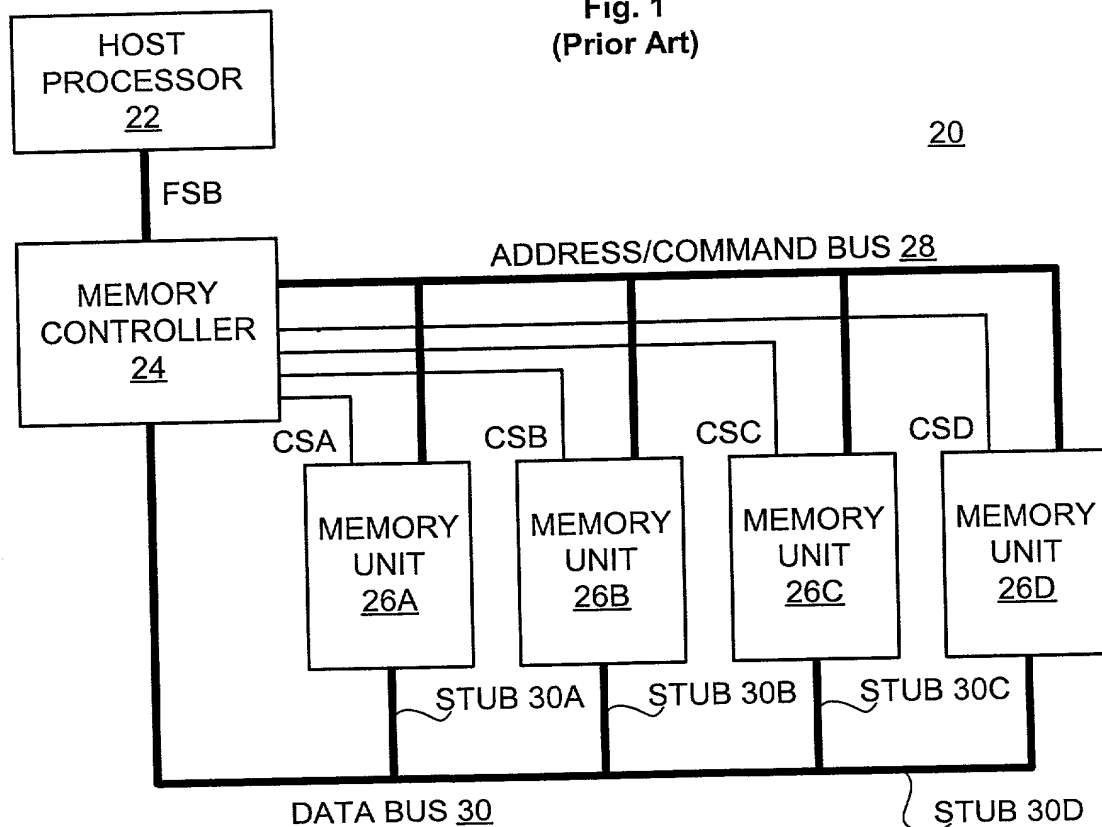
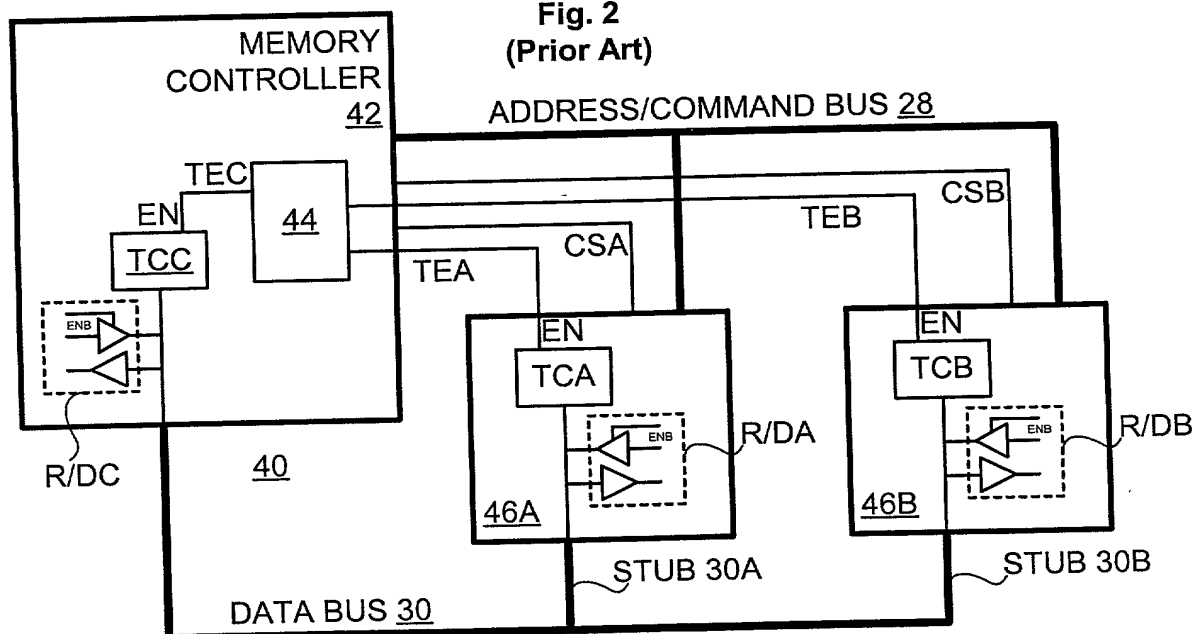


Fig. 2  
(Prior Art)



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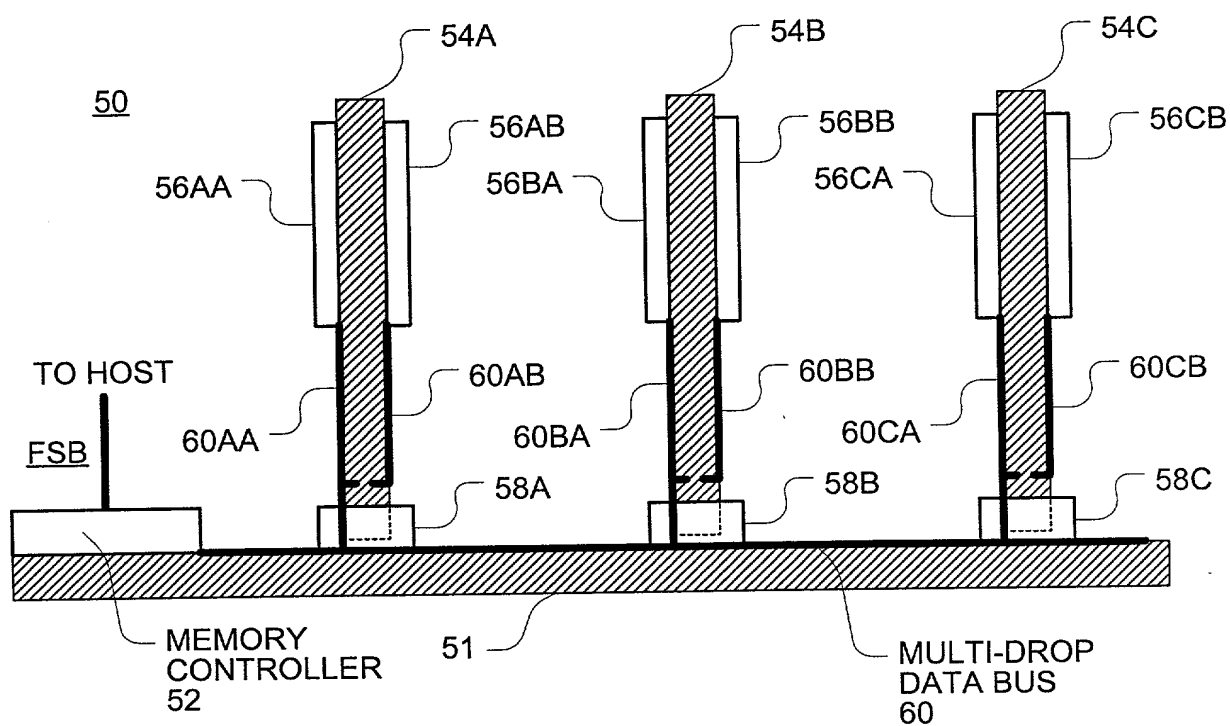
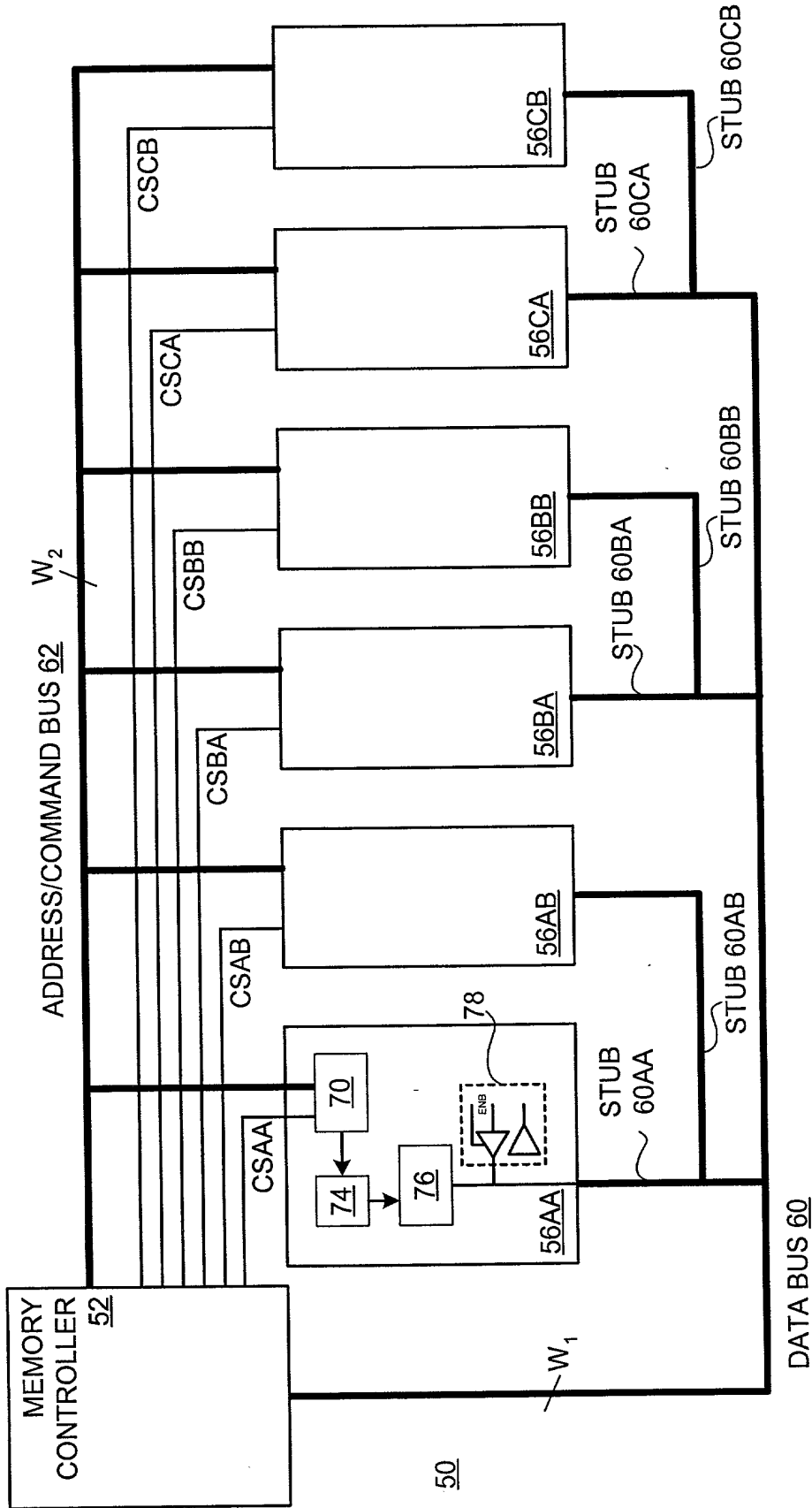


Fig. 3

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Fig. 4



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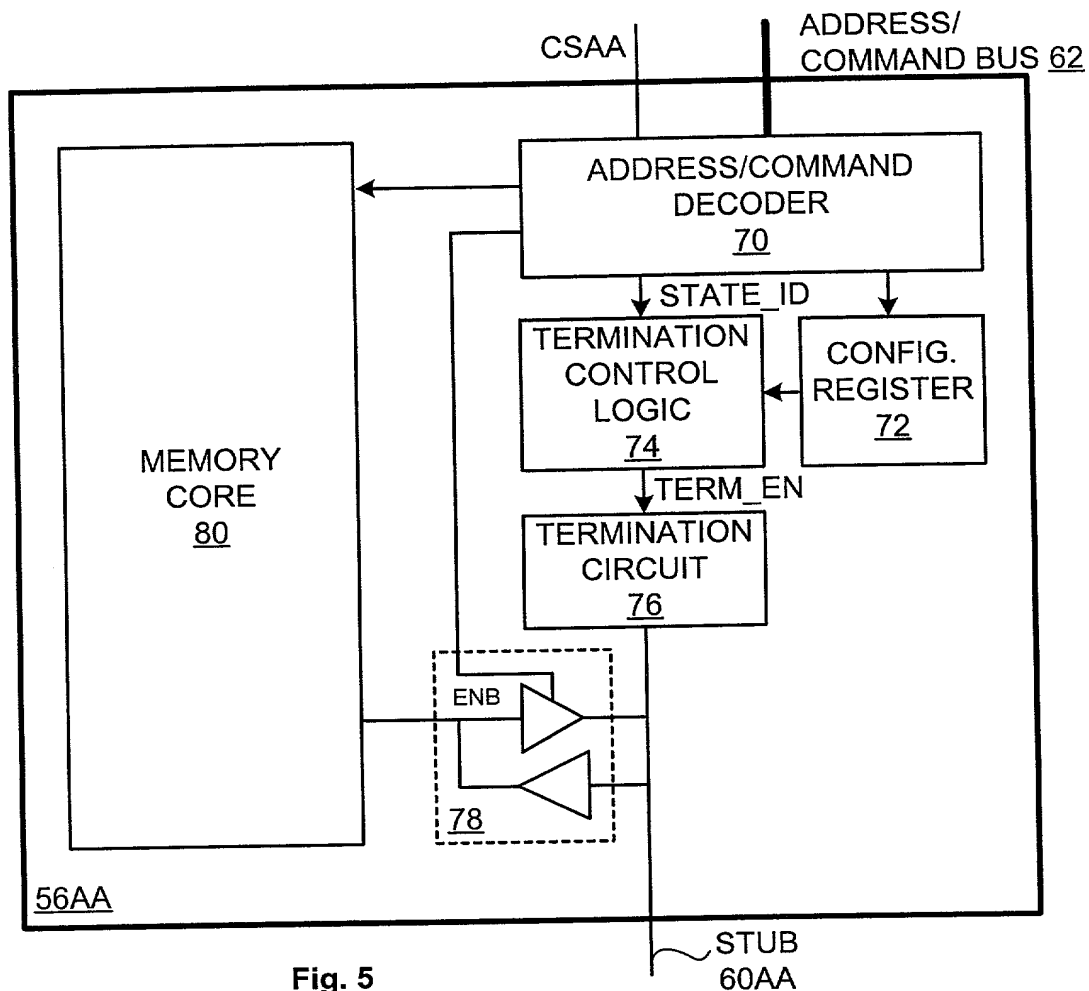


Fig. 5

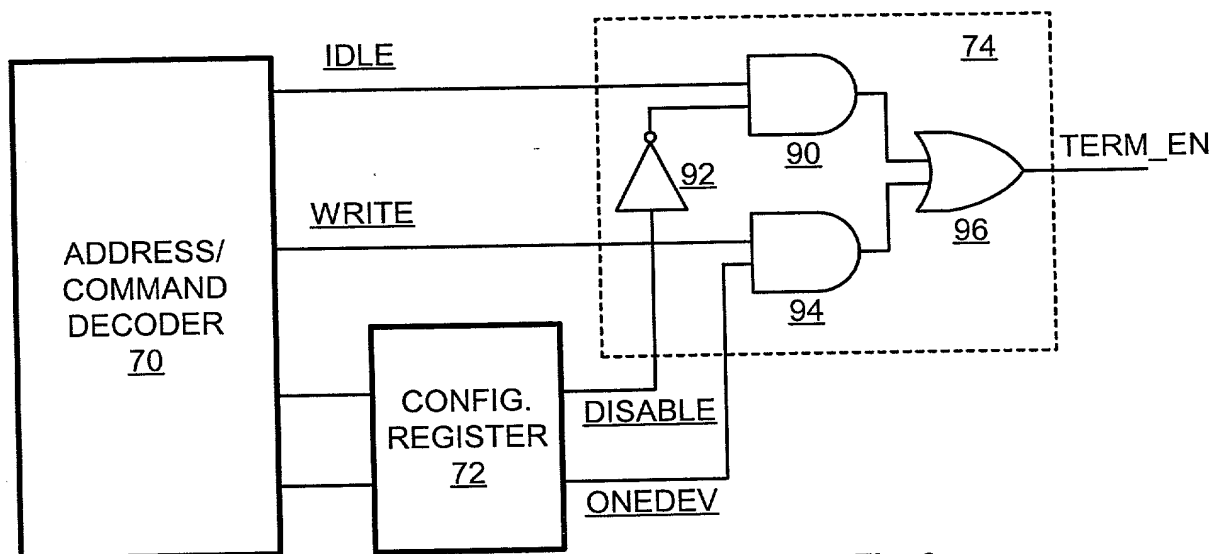


Fig. 6

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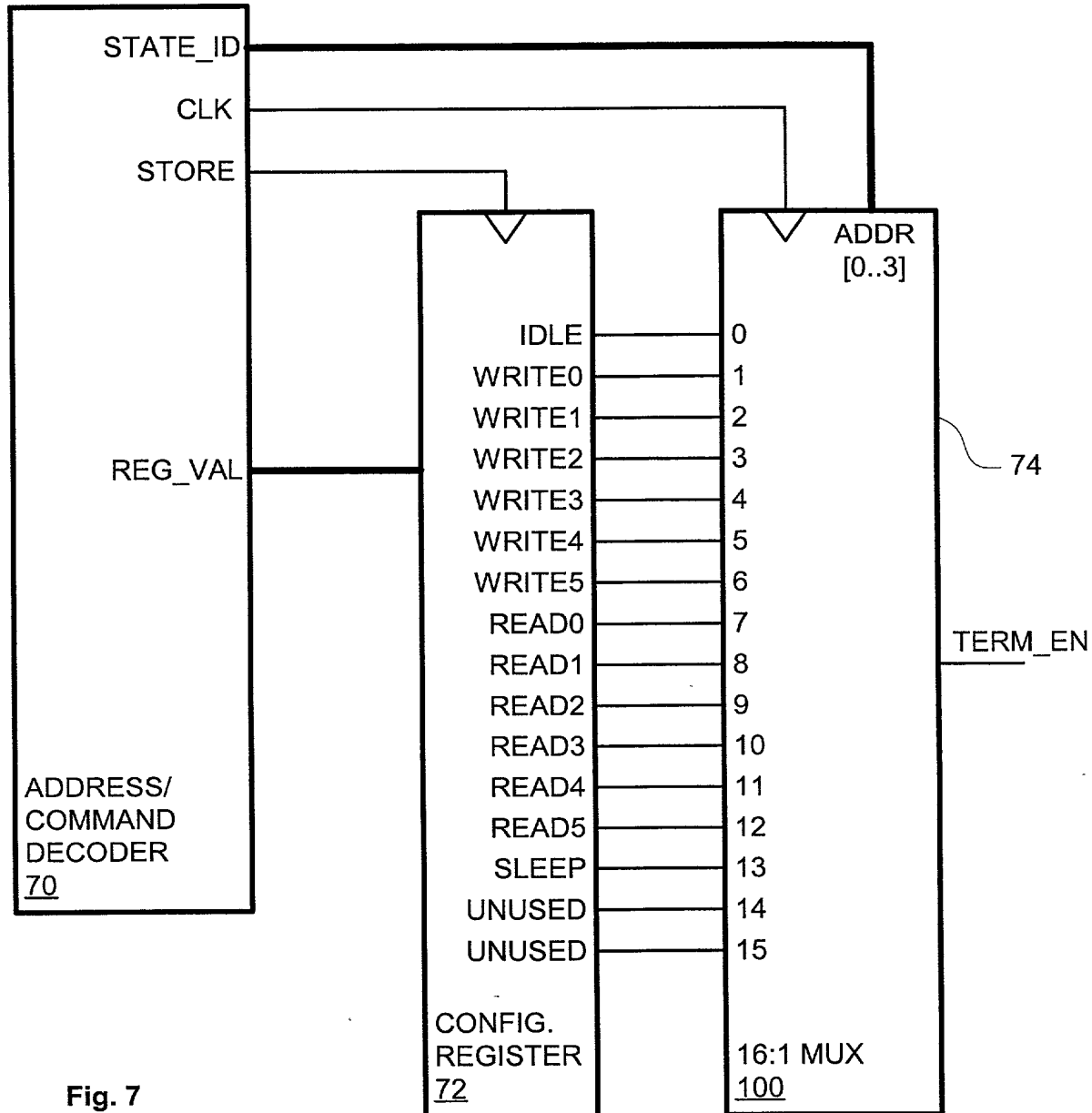


Fig. 7

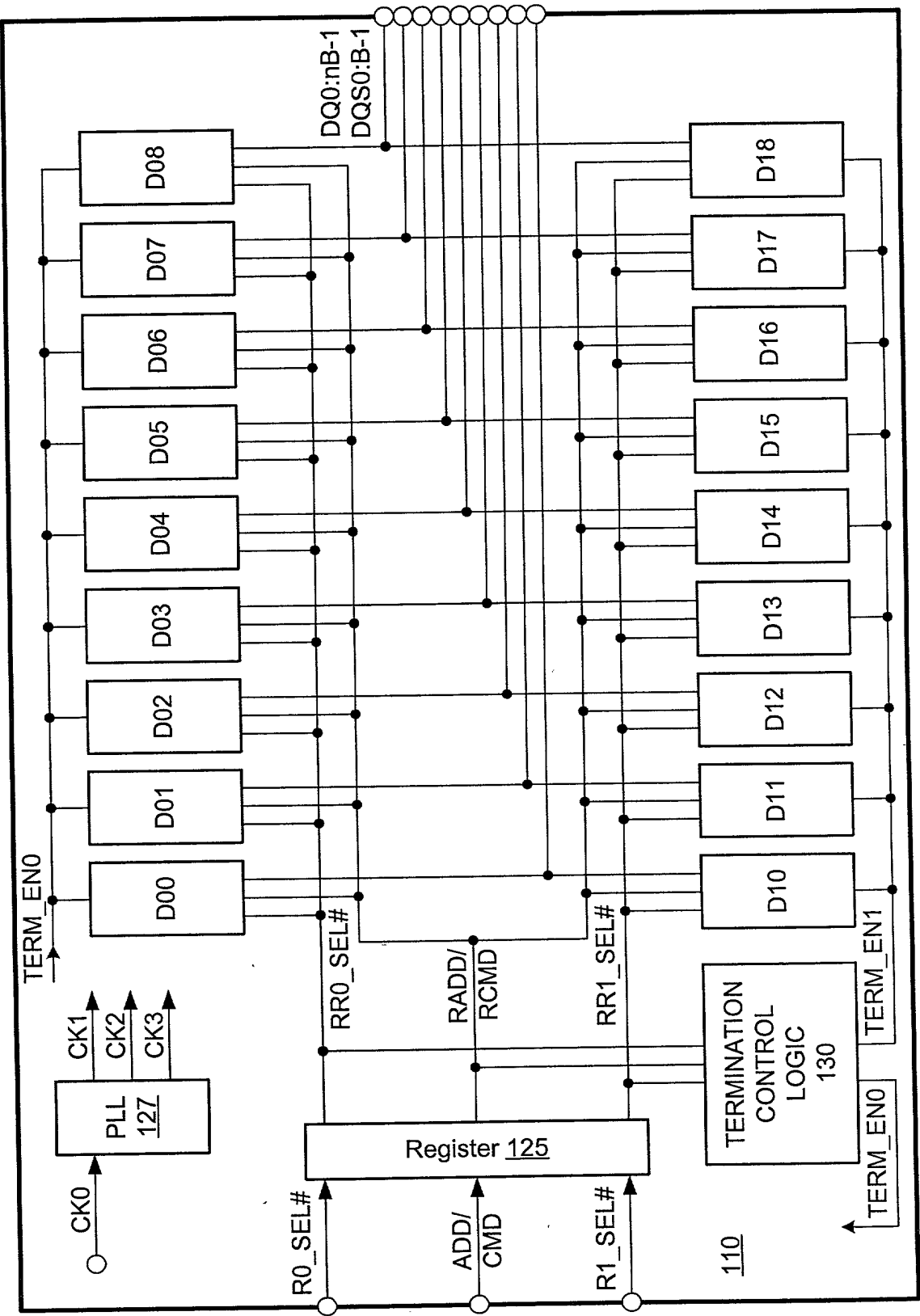


Fig. 8

FIG. 8 is a schematic diagram of a memory unit having termination control.